Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2	(("6737726") or ("6653193")).PN.	US-PGPUB; USPAT	OR	OFF	2005/06/29 14:39
L2	1	("20030127664").PN.	US-PGPUB; USPAT	OR	OFF	2005/06/29 14:42
L3	2	(("6410397") or ("6232648")).PN.	US-PGPUB; USPAT	OR	OFF	2005/06/29 14:46
L4	5	(analogous adj memory) and (second adj electrode)	US-PGPUB; USPAT	OR	ON	2005/06/29 14:47
L5	32	(analogous adj memory) and (electrode)	US-PGPUB; USPAT	OR	ON	2005/06/29 15:01
L6	260	(analogous near5 memory) and (electrode)	US-PGPUB; USPAT	OR	ON	2005/06/29 14:48
L7	163	6 and @ad<"20001208"	US-PGPUB; USPAT	OR	ON	2005/06/29 15:01
L8	701	(analog adj memory) and (electrode)	US-PGPUB; USPAT	OR	ON	2005/06/29 15:01
L9	347	(analog adj memory) and (second with electrode)	US-PGPUB; USPAT	OR	ON	2005/06/29 15:08
L10	227	9 and @ad<"20001208"	US-PGPUB; USPAT	OR	ON	2005/06/29 15:08
L11	213	10 not 7	US-PGPUB; USPAT	OR	ON	2005/06/29 15:02
L12	360	(analog$3 adj memory) and (second with electrode)	US-PGPUB; USPAT	OR	ON	2005/06/29 16:10
L13	237	12 and @ad<"20001208"	US-PGPUB; USPAT	OR	ON	2005/06/29 15:18
L14	213	13 not 7	US-PGPUB; USPAT	OR	ON	2005/06/29 16:53
L15	0	14 not 11	US-PGPUB; USPAT	OR	ON	2005/06/29 15:09
L16	235	(analog$3 adj memory) and ((upper or top) with electrode)	US-PGPUB; USPAT	OR	ON	2005/06/29 15:51
L17	115	16 and @ad<"20001208"	US-PGPUB; USPAT	OR	ON	2005/06/29 15:55
L18	108	17 not 7	US-PGPUB; USPAT	OR	ON	2005/06/29 15:19
L19	26	18 not 11	US-PGPUB; USPAT	OR	ON	2005/06/29 15:19
L20	33	(analog$3 adj memory) and ((second or upper or top) with electrode)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/29 15:53
L21	49551	(memory) and ((second or upper or top) with electrode)	US-PGPUB; USPAT	OR	ON	2005/06/29 15:54

L22	41435	21 and (opening or trench or aperture or recess or hole or via)	US-PGPUB; USPAT	OR	ON	2005/06/29 15:54
L23	35788	22 and (resistance or voltage)	US-PGPUB; USPAT	OR	ON	2005/06/29 15:55
L24	18878	23 and @ad<"20001208"	US-PGPUB; USPAT	OR	ON	2005/06/29 15:55
L25	5652	24 and analog$3	US-PGPUB; USPAT	OR	ON	2005/06/29 15:56
L26	2465	24 and (analog$3 same memory)	US-PGPUB; USPAT	OR	ON	2005/06/29 15:56
L27	2380	26 not 7	US-PGPUB; USPAT	OR	ON	2005/06/29 15:56
L28	2209	27 not 11	US-PGPUB; USPAT	OR	ON	2005/06/29 15:56
L29	2185	28 not 18	US-PGPUB; USPAT	OR	ON	2005/06/29 15:57
L30	2185	29 not 14	US-PGPUB; USPAT	OR	ON	2005/06/29 15:57
L31	1849	30 and current	US-PGPUB; USPAT	OR	ON	2005/06/29 15:58
L32	1468	31 and controlled	US-PGPUB; USPAT	OR	ON	2005/06/29 15:58
L33	514	31 and (controlled with (resistance or current))	US-PGPUB; USPAT	OR	ON	2005/06/29 15:58
L34	495	33 and set$4	US-PGPUB; USPAT	OR	ON	2005/06/29 16:05
L35	166	(terry with gilton)	US-PGPUB; USPAT	OR	ON	2005/06/29 16:10
L36	117	35 and (gate or electrode)	US-PGPUB; USPAT	OR	ON	2005/06/29 16:06
L37	90	36 and memory	US-PGPUB; USPAT	OR	ON	2005/06/29 16:06
L38	0	(terry with gilton)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/29 16:10
L39	126	(analog$3 adj memory) and (second with electrode) and micron	US-PGPUB; USPAT	OR	ON	2005/06/29 16:16
L40	74	39 and @ad<"20001208"	US-PGPUB; USPAT	OR	ON	2005/06/29 16:11
L41	3	(analog$3 adj memory) and (second with electrode) and micron	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/29 16:39

L42	18	(("3,622,319") or ("3,743,847") or ("4,269,935") or ("4,312,938") or ("4,320,191") or ("4,405,710") or ("4,419,421") or ("4499557") or ("4,795,657") or ("4,847,674") or ("5,177567") or ("5,219,788") or ("5,238,864") or ("5,315,131") or ("5,350,484") or ("5,360,981") or ("5,512,328") or ("5,512,773")).PN. or (2002/0168820).CCLS.	US-PGPUB; USPAT	OR	OFF	2005/06/29 16:58
L43	18	(("200200168820") or ("3,622,319") or ("3,743,847") or ("4,269,935") or ("4,312,938") or ("4,320,191") or ("4,405,710") or ("4,419,421") or ("4499557") or ("4,795,657") or ("4,847,674") or ("5,177567") or ("5,219,788") or ("5,238,864") or ("5,315,131") or ("5,350,484") or ("5,360,981") or ("5,512,328") or ("5,512,773")).PN.	US-PGPUB; USPAT	OR	OFF	2005/06/29 16:54
L44	1	("20020168820").PN.	US-PGPUB; USPAT	OR	OFF	2005/06/29 16:54
L45	18	(("5,726,083") or ("5,751,012") or ("5,761,115") or ("5,789,277") or ("5,841,150") or ("5,846,889") or ("6,388,324") or ("6,469,364") or ("5,896,312") or ("5,914,893") or ("5,920,788") or ("5,998,066") or ("6,077,729") or ("6,084,796") or ("6,117,720") or ("6,143,604") or ("6,177,338") or ("6,236,059")).PN.	US-PGPUB; USPAT	OR	OFF	2005/06/29 17:00
L46	13	(("6,297,170") or ("6,300,684") or ("6,316,784") or ("6,329,606") or ("6,348,365") or ("6,350,679") or ("6,376,284") or ("6,391,688") or ("6,414,376") or ("6,418,049") or ("6,423,628") or ("6,653,193") or ("6,638,820")).PN.	US-PGPUB; USPAT	OR	OFF	2005/06/29 17:03
L47	4	(("6,388,324") or ("5,500.532") or ("6,469,364") or ("6,635,914") or ("6,670,713")).PN.	US-PGPUB; USPAT	OR	OFF	2005/06/29 17:04
L48	2	(("5789277") or ("5751012")).PN.	US-PGPUB; USPAT	OR	OFF	2005/06/29 17:34
L49	2071	257/528-530,536.ccls.	US-PGPUB; USPAT	OR	ON	2005/06/29 17:37
L50	704	49 and memory and (gate or electrode)	US-PGPUB; USPAT	OR	ON	2005/06/29 17:49
L51	433	50 and @ad<"20001208"	US-PGPUB; USPAT	OR	ON	2005/06/29 17:49
L52	431	51 not 7	US-PGPUB; USPAT	OR	ON	2005/06/29 17:36

L53	425	52 not 14	US-PGPUB; USPAT	OR	ON	2005/06/29 17:36
L54	425	53 not 18	US-PGPUB; USPAT	OR	ON	2005/06/29 17:36
L55	415	54 not 30	US-PGPUB; USPAT	OR	ON	2005/06/29 17:38
L57	1464	257/209,245,330.ccls.	US-PGPUB; USPAT	OR	ON	2005/06/29 17:49
L58	579	57 and memory	US-PGPUB; USPAT	OR	ON	2005/06/29 17:49
L59	351	58 and @ad<"20001208"	US-PGPUB; USPAT	OR	ON	2005/06/29 17:49
L60	297	59 not 55	US-PGPUB; USPAT	OR	ON	2005/06/29 17:49

US-PAT-NO: 5989943

DOCUMENT-IDENTIFIER: US 5989943 A

TITLE: Method for fabrication of programmable interconnect structure

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Abstract Text - ABTX (1):

In one method for forming amorphous silicon antifuses with significantly reduced leakage **current,** a film of amorphous silicon is formed in a antifuse **via** between two electrodes. The amorphous silicon film is deposited using plasma enhanced chemical vapor deposition, preferably in an silane-argon environment and at a temperature between 200 and 500 degrees C., or reactively sputtered in a variety of reactive gases. In another method, an oxide layer is placed between two amorphous silicon film layers. In yet another method, one of the amorphous silicon film layers about the oxide layer is doped. In another embodiment, a layer of conductive, highly diffusible material is formed either on or under the amorphous silicon film. The feature size and thickness of the amorphous silicon film are selected to minimize further the leakage **current** while providing the desired programming **voltage**. A method also is described for for forming a field programmable gate array with antifuses.

Brief Summary Text - BSTX (5):

Programmable semiconductor devices include programmable read only **memories** ("PROMs"), programmable logic devices ("PLDs"), and programmable gate arrays. Programmable elements suitable for one or more of these device types include fuses and antifuses.

Brief Summary Text - BSTX (6):

A fuse is a structure which electrically couples a first terminal to a second terminal, but which, when programmed by passage of sufficient **current** between its terminals, electrically decouples the first terminal from the second terminal. A fuse typically is of a conductive material which has a geometry that causes portions of the conductive fuse material to physically separate from each other when heated to the extent that an open circuit results.

Brief Summary Text - BSTX (7):

An antifuse is a structure which when unprogrammed does not electrically couple its first and second terminals, but which, when programmed by applying sufficient **voltage** between the first and second terminals, permanently electrically connects the first and second terminals. One type of antifuse comprises a highly resistive material between two terminals of conductive material, the antifuse material being such that when sufficient **voltage** is applied, the resulting **current** heats the materials and causes portions of the conductive material to extend into the resistive material and form a permanent conductive path. Another type of antifuse comprises an amorphous silicon which forms conductive polysilicon when heated. In PROM devices, for example, the advantages of the antifuse technology over fuse technology include scalability and reduced programming **current** requirement. Various antifuses are disclosed in U.S. Pat. No. 3,675,090, issued Jul. 4, 1972 to Neale, and U.S. Pat. No. 3,792,319, issued Feb. 12, 1974 to Tsang.

Brief Summary Text - BSTX (8):

The use of amorphous silicon in the fabrication of semiconductor threshold and switch devices is well known. As more fully discussed in the aforementioned Neale patent, various semiconductor switch devices comprise a "pore" filled with amorphous silicon, which contacts a lower **electrode** forming surface and an **upper electrode** forming surface. The **electrodes** are variously described as comprising a refractory material alone (Neale, FIG. 4), a refractory material connected at its **upper** surface to an aluminum conductor (Neale, FIG. 6), a refractory material overlaying an aluminum conductor (Neale, FIGS. 8-9), and a refractory material connected at its end to an aluminum conductor (Neale, FIG. 11).

Brief Summary Text - BSTX (9):

Neale recognized that two important objectives were to obtain switch devices with a very low leakage **current** in the preprogrammed condition and a fairly consistent programming **voltage** value. An aspect of the Neale invention was to fabricate the semiconductor switch device so as to present a very small cross-sectional area of semiconductor material for **current** flow to minimize leakage **current** paths therethrough. Unfortunately, these measures alone are insufficient to achieve low leakage **current** along with a low and consistent programming **voltage,** which is desired in many applications.

Brief Summary Text - BSTX (10):

Antifuses have been used successfully in programmable interconnect substrates, **memories,** and some types of PLDs.

Brief Summary Text - BSTX (11):

An antifuse suitable for use in an electrically programmable interconnection substrate is disclosed in U.S. Pat. No. 4,458,297, issued Jul. 3, 1984 to Stopper et al. A silicon substrate for hybrid circuits is divided into discrete areas for hosting integrated circuit chips and providing the bonding pads for the signal connections between the chips and the substrate. Transverse pad lines and net lines are provided, which are insulated at the crossover points except for respective **via holes,** each furnished with a pad of amorphous silicon material. The lines are arranged so that a number of pads can be connected to each other as desired by programming. See also Herbert Stopper, "A Wafer with Electrically Programmable Interconnections," in Proceedings of the International Solid State Circuits Conference, Feb. 15, 1985, pp. 263-269.

Brief Summary Text - BSTX (12):

Antifuses used in interconnect substrates tend to require high programming **voltages and currents**. As the interconnection substrate does not contain sensitive integrated active semiconductor devices, and as programming is completed prior to attachment and bonding of the functional die, the antifuses between the pad and net lines are designed to minimize the leakage **current,** and do not minimize the programming **current** and programming **voltage**.

Brief Summary Text - BSTX (13):

Specifically, the device described by Stopper requires that a threshold **voltage** of 20 volts be exceeded to initiate the switching process into the programmed state. Many devices designed to operate at 5 volts (the typical integrated circuit operating **voltage**) cannot tolerate **voltages** as high as 20 volts due to junction breakdown **voltages** between 12-20 volts. Although higher junction breakdown **voltages** can be obtained in integrated circuits, thicker insulation layers throughout the circuit, larger transistors, lower doping levels, and other component adjustments must be provided. These changes cause a reduction in the operating frequency as well as an increase in the size of the circuit. Thus a higher breakdown **voltage** is accompanied by a direct trade-off in circuit performance.

Brief Summary Text - BSTX (15):

In the **via** antifuse of FIG. 1, first metal comprising aluminum conductor 14 and barrier metal 10 and 11 is provided on an oxide layer 13 overlaying substrate 12. A thick oxide layer 18 is provided over conductor 14 as insulation from second metal. A **via** etched into oxide layer 18 is lined with a thin film of amorphous silicon 15, which fully overlays and contacts the barrier metal 11 under the **via**. Second metal comprising barrier metal 16 and aluminum conductor 17 is provided over the **via,** in contact with the amorphous silicon 15.

Brief Summary Text - BSTX (16):

The contact antifuse of FIG. 2 is formed over a transistor comprising collector 20, base 21, and emitter 22. Emitter contact is made to a platinum silicide region 23 through a contact **hole** in oxide 24, which is lined with amorphous silicon film 25. Barrier metal 26 and aluminum conductor 27 overlay the amorphous silicon 25, and are protected by oxide 28.

Brief Summary Text - BSTX (17):

In the examples of FIGS. 1 and 2, the deposition of the amorphous silicon was a critical step in the process, as the thickness of the film 15 (FIG. 1) and film 25 (FIG. 2) was thought to control the programming **voltage**. The pre-programmed leakage **current** was reduced to about 6 microamperes at 2 volts by a high temperature anneal at 450 degrees C. Other factors thought to influence leakage **current** in the undoped amorphous silicon antifuse were feature size (leakage **current** proportional) and film thickness (leakage **current** inversely proportional).

Brief Summary Text - BSTX (18):

Unfortunately, antifuse technology developed for use in **memories** is generally too leaky for use in PLDs, as noted by Cook et al. In a PROM, one bit is selected per output at a time; therefore, if the programmable elements are leaky, only one leaky bit loads the sense amplifier. Usually the sense amplifier can tolerate this loading without drastically affecting its functionality or performance. Contrast one type of PLD known as a programmable array logic, which is implemented using PROM technology. The programmable elements are used to configure logic (routing is dedicated and global). In programmable array logic, multiple bits can be accessed and may overload the sense line if the programmable elements are leaky. Overloading the sense line may drastically degrade the performance and in the extreme case, result in functional failure.

Brief Summary Text - BSTX (19):

Certain techniques have been employed in PLDs using antifuse technology to overcome the problems created by antifuse leakage. One technique uses active semiconductor devices such as diodes or transistors to block the leakage **current,** an approach which can also be used in **memories** having leaky antifuses. While this approach is satisfactory in **memories** and in the logic configuration circuits of PLDs, the technique is not satisfactory for use in the routing circuits of such integrated circuits as the field programmable gate array ("FPGA").

Brief Summary Text - BSTX (20):

The FPGA, which is distinguished from conventional gate arrays by being user programmable, otherwise resembles a conventional gate array in having an interior matrix of logic blocks and a surrounding ring of I/O interface blocks. Logic functions, I/O functions, and routing of interconnect networks are all user configurable, which affords high density and enormous flexibility suitable for most logic designs. User logic, for example, conventionally is implemented by interconnecting two-input NAND gates into more complex functions. Extensive user configurability of the FPGA is achieved by incorporating a large number of programmable elements into the logic and I/O blocks and the interconnect network. Naturally, the leakage requirement of the programmable elements is stringent, due to the large number of possible connections generally involved and the numerous failure modes that leakage can cause. For instance, leaky programmable elements in the routing areas contribute to high supply **current** problems, cross talk problems, and performance degradation.

Brief Summary Text - BSTX (21):

To meet the stringent leakage requirements imposed by FPGAs, conventional fuses and transistor switches generally have been employed. Antifuses using amorphous silicon have not been employed due to their excessive leakage when designed for the programming **voltages and currents** conventionally used in FPGAS.

Brief Summary Text - BSTX (23):

Some embodiments of the amorphous silicon antifuses of the present invention offer a low leakage **current** while requiring programming **voltages, currents,** and time compatible with such devices as field programmable gate arrays.

Brief Summary Text - BSTX (24):

Some embodiments of the amorphous silicon antifuses of the present invention combine an operating **voltage** of 5 to 5.5 volts with a programming **voltage** above 10 volts but under 20 volts.

Brief Summary Text - BSTX (25):

These and other advantages are achieved in the present invention, a method for fabricating a programmable interconnect structure for an integrated circuit. The method generally includes the steps of fabricating a first conductor; fabricating an insulating layer overlaying the first conductor; fabricating an **opening** through the insulating layer at a selected location and terminating the **opening** at a portion of the first conductor; forming a layer of an antifuse material; patterning the antifuse material to form at the selected location an antifuse feature substantially restricted to the **opening,** the

feature having a region contacting and fully overlaying the first conductor portion; and fabricating a second conductor, wherein a portion of the second conductor contacts and overlays the amorphous silicon region. In one embodiment, the antifuse material is amorphous silicon, deposited using either plasma enhanced chemical vapor deposition or reactive ion sputtering. In another embodiment, the antifuse material includes a layer of a conductive, highly diffusible material formed either on or under the amorphous silicon film. In yet another embodiment of the present invention, the antifuse material includes a dielectric layer formed between two layers of amorphous silicon film. In a variation of this embodiment, one of the silicon layers is doped.

Drawing Description Text - DRTX (6):

FIG. 9 is a graph illustrating **current voltage** characteristics of an antifuse fabricated in accordance with the present invention.

Detailed Description Text - DETX (3):

The antifuses illustrated in FIGS. 3-6 include a semiconductive substrate (not shown), a dielectric layer 32, a first conductive layer 33, a second conductive layer 36, a dielectric layer 34 including **via** 39, and an amorphous silicon structure 35 extending into **via** 39 and contacting both the first conductive layer 33 and the second conductive layer 36. The first dielectric layer 32, typically silicon dioxide, is patterned to expose substrate 31, typically silicon, at locations where portions of first conductive layer 33, typically polycrystalline silicon or aluminum, contact substrate 31. Likewise **vias such as via** 39 are formed in second dielectric 34, also typically silicon dioxide, where first conductive layer 33 is to be exposed. Antifuses may be formed in some such **vias** of the integrated circuit and not in other **vias**.

Detailed Description Text - DETX (4):

The following basic steps are used in the process for forming an antifuse of this invention. A layer of dielectric 32, typically silicon dioxide, is formed on the silicon substrate, and patterned to expose portions of the substrate 31. Alternatively, the dielectric layer 32 may be formed upon a lower conductive layer (not shown) rather than to substrate 31. A first conductive layer 33 of, for example, aluminum or polycrystalline silicon, is formed on the dielectric 32. First conductive layer 33 is patterned to form appropriate interconnects. A second layer of dielectric 34, again typically silicon dioxide, is formed on the first conductive layer 33 and patterned to form **vias such as via** 39 exposing first conductive layer 33. Some of these **vias,** in particular **via** 39, will serve as sites for antifuses. Other **vias,** not shown, may allow for direct connection between first conductive layer 33 and a to-be-formed second

conductive layer 36.

Detailed Description Text - DETX (5):
Into those **vias** which will have antifuses is formed the antifuse structure 35, as will be discussed. The antifuse material may extend somewhat beyond the edge of the **via** 39 which it fills. Next, second conductive layer 36, typically a metal such as aluminum, is applied and patterned, followed by application and patterning of a final passivation layer (not shown), typically a silicon oxide or silicon nitride.

Detailed Description Text - DETX (6):
Generally, the antifuses of FIGS. 3-6 are particularly advantageous for applications which require that the antifuse reliably does not program at a **voltage** below 7.5 volts and reliably programs at a **voltage** above 10 volts. The range between 7.5 volts and 10 volts is a guard band. Such applications also require that the antifuses pass very little **current** until programmed; leakage across the antifuses prior to programming of less than 10 nanoamperes at 5.5 volts is desirable.

Detailed Description Text - DETX (8):
The antifuse structure 35 shown in FIG. 3 is a layer of amorphous silicon film. At this point, several process and structural parameters can be identified as important, especially for amorphous silicon antifuses designed for use in FPGAs and other integrated circuit applications sensitive to leakage **current**. These parameters influence important characteristics of the antifuse, including trigger **current (current** at initiation of the programming mechanism), programming **voltage (voltage** at initiation of the programming mechanism), programming **current (current** provided to form electrical connection upon which the programmed **resistance** depends), programming time (period over which the programming **current** is maintained), leakage **current,** and reproducibility of the structure (necessary to maintain high yield).

Detailed Description Text - DETX (9):
The programming **voltage** is controlled by the thickness of the amorphous silicon film 35 in contact with the conductor 33 at the bottom of the antifuse **via** 39. Film 35 is deposited to a thickness of about 2000 Angstroms, which results in a programming **voltage** of about 12 volts. Of course, other programming **voltages** may be achieved by depositing film 35 to an appropriate thickness. The leakage **current is controlled** by several factors, including feature size and film thickness. Feature size and film thickness are selected to minimize leakage **current,** consistent with the process used and the programming **voltage** desired. In the present embodiment, the feature size is

US-PAT-NO: 5365097

DOCUMENT-IDENTIFIER: US 5365097 A
See image for Certificate of Correction

TITLE: Vertical epitaxial SOI transistor, memory cell and fabrication methods

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Detailed Description Text - DETX (21):
Functionally device 50 is **analogous to memory** cell 11 described in connection with FIGS. 2-6. However, as will be apparent from the following fabrication discussion, the memory cell embodiment of FIG. 7 provides significantly improved leverage to contain the node diffusions within the vertical trench 66. For example, the extent of first node diffusion 78 is more easily and exactly controlled, as is the thickness of monocrystalline epitaxial material 82 on the vertical sidewall of trench 66. By the provision of relatively thick spacer oxides about first node diffusion 78 capacitive coupling between this diffusion and the gate is also limited.

Detailed Description Text - DETX (49):
Dual storage node 208 includes a central plug 212 which is in electrical contact with substrate 202 at the bottom surface of trench 206. Assuming substrate 202 has a P+ conductivity, then plug 212 comprises polysilicon material having a P+ conductivity doping. The capacitor's storage **electrode** 214 is isolated from inner trench plug 212 by a first dielectric material 216 and is isolated from substrate 202 by a **second** dielectric material 218. A dielectric cap 220 isolates inner storage plate 212 from the field effect transistor disposed in the upper portion of trench 206.

Claims Text - CLTX (1):
1. A vertical transistor formed in a substrate and one or more isolation layers overlying said substrate, said transistor comprising a trench in said substrate and said one or more isolation layers, said trench including a trench sidewall, said transistor residing entirely within said trench and having a gate **electrode** and a bulk channel proximate thereto within which an inversion layer is formed when said gate **electrode** is appropriately biased, said bulk channel being disposed directly on said trench sidewall and electrically connected to said substrate for receiving a back biasing potential through said

substrate, said transistor also including a first node diffusion and a **second** node diffusion, said first node diffusion being disposed at an upper end of said bulk channel and said **second** node diffusion being disposed at a lower end of said bulk channel, said node diffusions being contained within said trench.

Claims Text - CLTX (22):

22. A vertical transistor formed in a substrate and one or more isolation layers overlying said substrate, said transistor comprising a trench in said substrate and said one or more isolation layers, said trench including a trench sidewall, said transistor residing entirely within said trench and having a gate **electrode** and a bulk channel proximate thereto within which an inversion layer is formed when said gate **electrode** is appropriately biased, said bulk channel being disposed directly on said trench sidewall and electrically connected to said substrate for receiving a back biasing potential through said substrate, said transistor also including a first node diffusion and a **second** node diffusion, said first node diffusion being disposed at an upper end of said bulk channel and said **second** node diffusion being disposed at a lower end of said bulk channel, said node diffusions being contained within said trench and said transistor further including a multi-layer sidewall spacer separating said first node diffusion from said gate **electrode** for reduced capacitance therebetween.

Claims Text - CLTX (23):

23. A memory cell formed in a substrate and one or more isolation layers overlying said substrate, said memory cell comprising a trench in said substrate and said one or more isolation layers, said trench having a sidewall, and an upper portion and a lower portion, a capacitive storage node formed in the lower portion of the trench and an access transistor formed in the upper portion of the trench, said access transistor having a gate **electrode** and a bulk channel proximate thereto within which an inversion layer is formed when said access transistor is appropriately biased, said bulk channel being disposed directly on said trench sidewall and electrically connected to said substrate for receiving a back biasing potential through said substrate, said access transistor also including a first node diffusion and a **second** node diffusion, said first node diffusion being disposed at an upper end of said bulk channel and said **second** node diffusion being disposed at a lower end of said bulk channel, said access transistor further including a multi-layered dielectric isolating said first node diffusion from said gate **electrode,** said multi-layered dielectric being fabricated so as to reduce overlap capacitance between said first node diffusion and said gate **electrode**.